IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE)
e-ISSN: 2278-1676,p-ISSN: 2320-3331, Volume 11, Issue 4 Ver. I (Jul. – Aug. 2016), PP 44-49
www.iosrjournals.org

Twenty Five Level Inverter by Cascading Of Two Transformers for AC Drives

Dr B Meenakshi1, Rahul Kumar2, R.Ramprakash3
[1](Professor,Electrical & Electronics Engineering, Sri Sairam Engineering College, India)
[2,3](Electrical & Electronics Engineering, Sri Sairam Engineering College, India)

Abstract : *In this paper, a new topology for 25-level cascaded inverter (H-bridge type) is proposed. In comparison to the 15-level cascaded inverter, which uses multiple DC sources for each basic unit and a total of 12 switches for the overall topology, the proposed topology for the H-bridge type 25-level inverter has a single DC source and the switches reduced to 10 (8 unidirectional and 2 bidirectional). Lossless transformers of specific turns ratios 1:1 and 1:5 are employed to obtain proper voltage levels on the output side. With the reduction in number of DC sources and switches in the proposed topology, a quality waveform with the appropriate number of levels is obtained. As a result, the Total Harmonic Distortion (THD) obtained is 5.92% as compared to 12.71% obtained for 15-level. Simulation and experimental results are provided to verify the performance and feasibility of the proposed topology.*

Keywords: *Cascaded inverter, lossless transformers, Total Harmonic Distortion (THD)*

I. Introduction

Till date, there has been immense research in proposing new topologies for cascaded multi-level inverter in order to realize their practical implementation in AC drive systems. The multi-level inverter comprises of three types, viz. diode clamped, flying capacitor and cascaded H-bridge inverter. Owing to the presence of difference voltage levels and suitability of power switches to adapt to these voltage levels for higher dv/dt protection makes these types of inverter widely popular. The existing topology of the 15-level inverter has higher THD content owing to the presence of multiple DC sources and switches in each basic circuitry used for cascading purpose. On the contrary, the proposed 25 level cascaded H-bridge type inverter has a single DC source and reduced number of switches with a much magnified output waveform.

II. Existing Topology

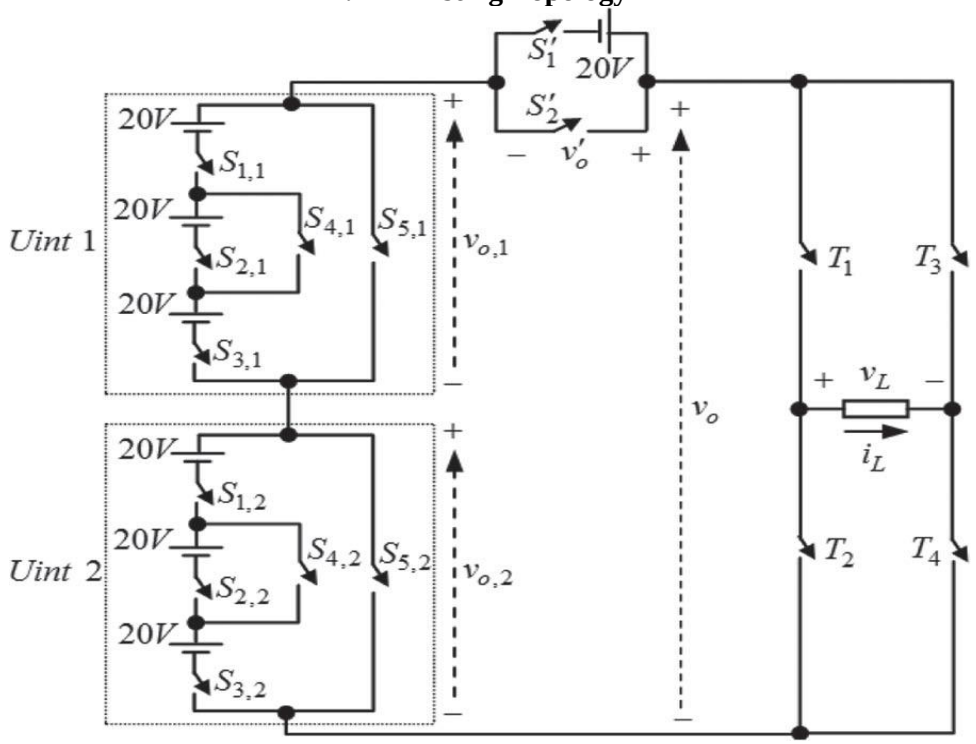

Fig 1: Existing topology

This existing model of 15-level inverter comprises of three dc voltage sources and five unidirectional power switches with the basic unit able to generate three different levels of 0, (V1+V3) and (V1+V2+V3) on the output side. It's important to note that the basic unit is only able to generate positive levels on the output. As this inverter is able to generate all voltage levels except V1, it is necessary to use an additional dc voltage source with the amplitude of V1 and two unidirectional switches that are connected in series with the proposed units. The graph showing the THD for the 15-level inverter is shown below:

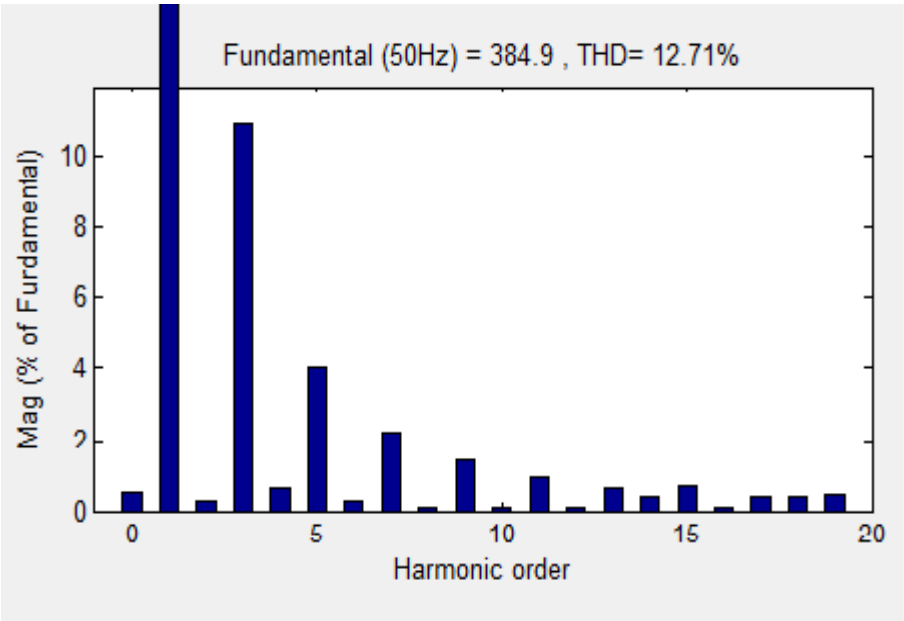

Fig 2: FFT analysis of 15-level inverter

III. Proposed Topology (25-Level Inverter Topology)

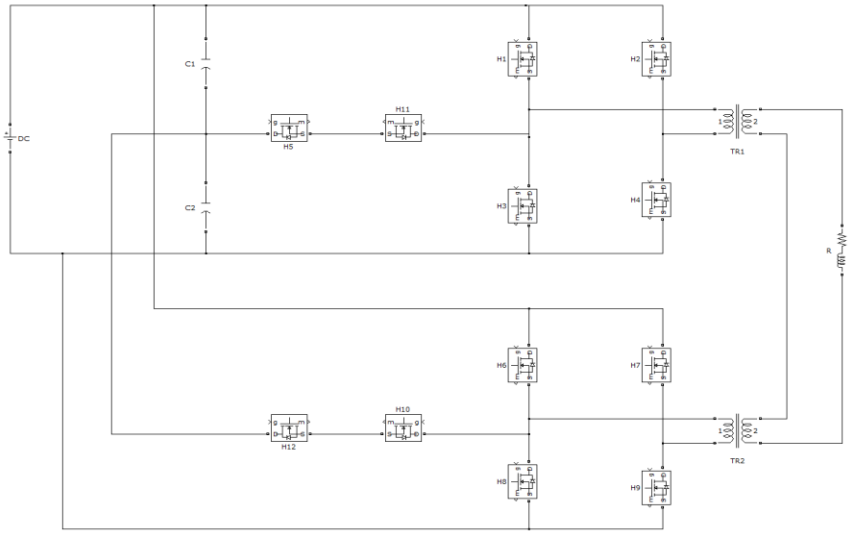

Fig 3: Proposed topology

The proposed topology contains two H-Bridges connected to a common DC Source. The bidirectional switches in the form of two MOSFETs are used in the cascading circuit to conduct both positive and negative voltage levels. Since the same gate pulse is given to both the MOSFETs in each cascading circuit, these pair of MOSFETs is considered as a single switch. Voltage splitting capacitors with specific ratings are used to increase the voltage level in steps of V/2 to obtain 12 positive and 12 negative levels. Two transformers of specific turns ratio 1:1 and 1:5 are cascaded to obtain the maximum voltage of six times the source voltages in steps of V/2. To verify the experimental results, the output parameters are measured across the power resistor 100 kilo-ohms. The micro-controller (AT-89C51) is programmed using ASM language to trigger the switches using gate pulses. The switching sequence for the proposed 25-level inverter is as follows:

	0	4	8	12	16	20	24	28	32	36	40	44	48	44	40	36	32	28	24	20	16	12	8	4	0
S_1	1	0	1	0	0	1	0	1	0	0	1	0	1	0	1	0	0	1	0	1	0	0	1	0	1
S_2	1	0	0	1	0	1	0	0	1	0	1	0	1	0	1	0	1	0	0	1	0	1	0	0	1
S_3	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0
S_4	0	1	1	0	0	0	1	1	0	0	0	1	0	1	0	0	0	1	1	0	0	0	1	1	0
S_5	1	1	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	1	1
S_6	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
S_7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S_8	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0
S_9	0	1	0	0	1	0	1	0	0	1	0	1	0	1	0	1	0	0	1	0	1	0	0	1	0
S_{10}	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0

Table 1: Switching pattern for positive half cycle (Assuming source voltage to be 8 V).

Similarly the 25 level is achieved by controlling the ON/OFF status of input voltage in positive half cycle the remaining level wiil be obtained by controlling the sequence in reverse direction.

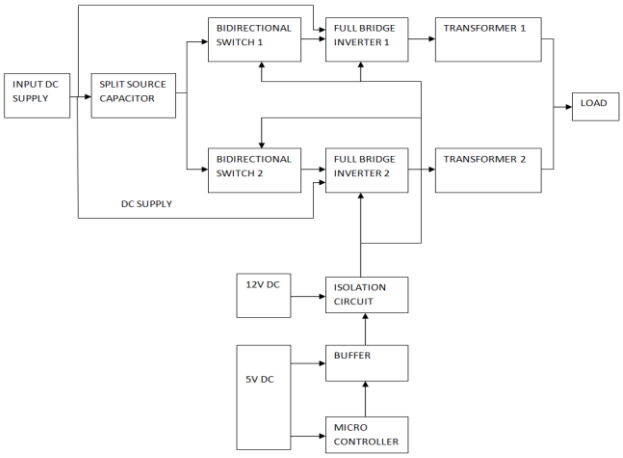

Fig 4: Block Diagram

The proposed design comprises of a H-bridge inverter, two bidirectional switches and a capacitor voltage divider formed by c1 & c2. The H-bridge topology is significantly advantageous over other topologies, i.e. less power switches, power diodes and capacitors for the inverters of the same number of levels. The bidirectional switch on the cascading circuitry eliminates the usage of additional switches. The modified circuit makes use of a single DC source but strives to achieve twenty five level inverter by means of efficient PWM technique and proper switching sequence pattern generated in the micro controller used. The gate pulses to these 10 switches should be configured effectively in such a manner that only one voltage level persists at any instant of time. Simulation and experimental data are compared with that of the 15-level proposed topology and the quantum of harmonics is measured using the THD analyser to check for permissible limits.

IV. Experimental Results

In order to verify the validity of the proposed topology necessary simulations were done using the MATLAB software. Following is the simulation circuit diagram for the proposed topology of the 25-level inverter:

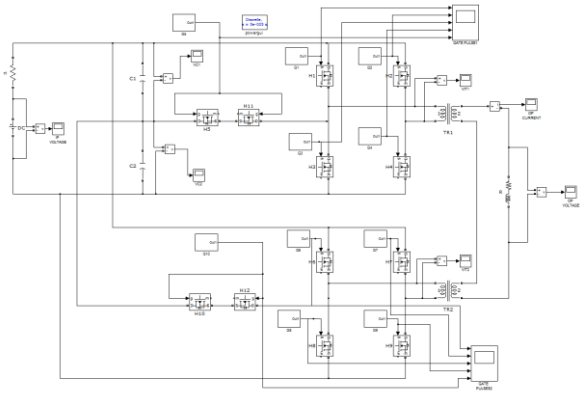

Fig 5: Proposed Simulation

Assuming the source voltage of 80 V, the maximum peak to peak staircase voltage varies from -480 V to +480 V in steps of V. This is achieved by cascading the voltage output from two H-bridge inverters using 1:1 isolation transformer and 1:5 step up transformer. Flexibility of using the two transformers of such varied transformation ratio helps in producing more voltage levels by virtue of algebraic summation of outputs. Bidirectional switches are simulated by having two MOSFET's connected in anti-parallel direction. The main purpose of using a bidirectional switch is to allow conduction of both positive and negative levels. Gate pulses to the MOSFET's are given using the Pulse Width Modulation technique.
The theoretical plots for the proposed topology are shown below:

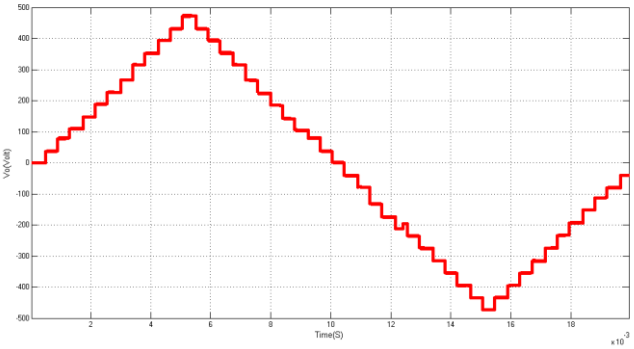

Fig 6: Output Voltage

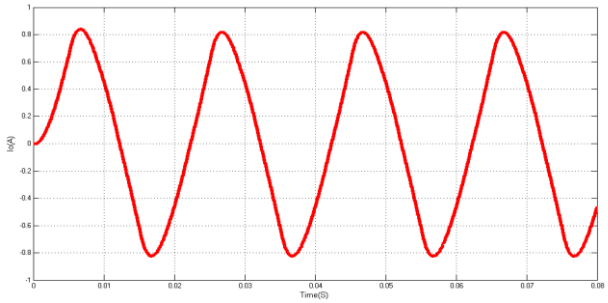

Fig 7: Output Current

The triggering pulses given across the gating circuits are shown in Figs 7.1 and 7.2.

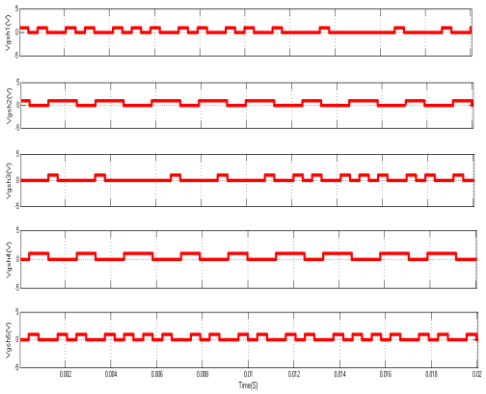

Fig 7.1 Triggering Pulses for switches S1-S5

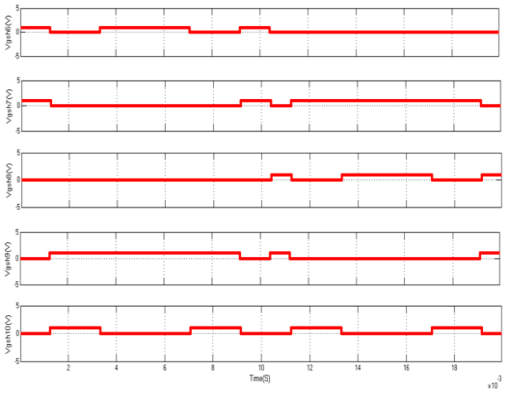

Fig 7.2. Triggering Pulses for switches S6-S10

The plot showing the THD after the FFT analysis is shown below:

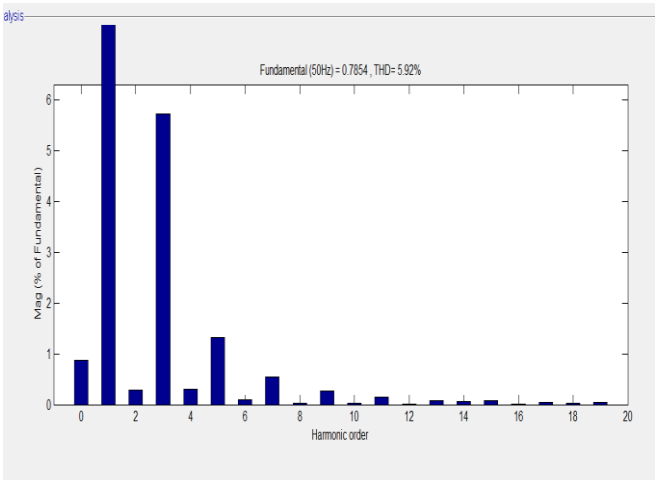

Fig 8: FFT analysis of proposed model

Hardware implementation of the proposed topology is shown:

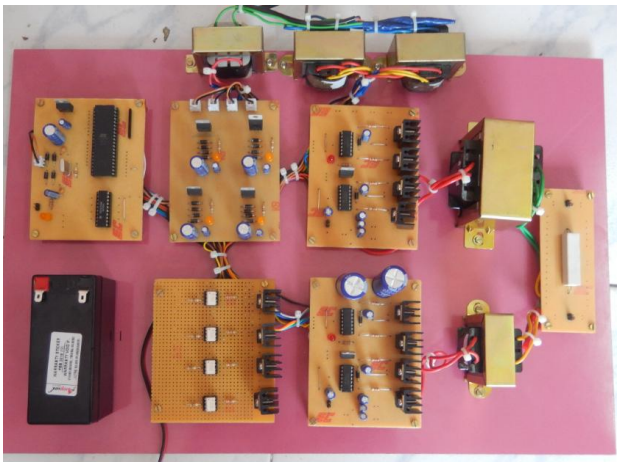

Fig 9: Hardware kit

The practical output as seen on the oscilloscope is as follows:

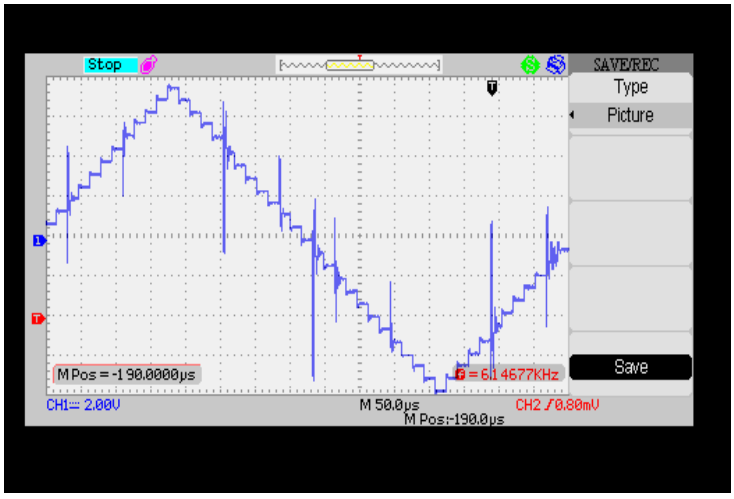

Fig 10: Twenty five level output

The disturbances in the plot shows that the system is trying to achieve a sinusoidal output wave.

V. Conclusion

In this paper a novel 25-level inverter is proposed. Compared to the conventional cascaded level inverter, the proposed model has lesser number of sources and switches. With the exponential increase in the number of voltage levels, the harmonics are significantly cut down in staircase output, which is particularly remarkable due to simple and flexible circuit topology. The Total Harmonic Distortion (THD) was found to be 5.92% which was far lesser than the 12.71% of the conventional type 15-level inverter. The proposed inverter can be applied to grid-connected photo-voltaic system and electrical network of EV.

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